

Claims 8, 18, 20, and 28 are amended as indicated by a marked up version of the rewritten claims, which follows the remarks, showing all the changes relative to the previous version of the claims:

FIG. 10

Clean Version of the Entire Set of Pending Claims

1 1. An apparatus comprising:

2 a storage circuit coupled to a prefetcher to store a plurality of
3 prefetch addresses, the plurality of prefetch addresses
4 corresponding to most recent access requests from a processor,
5 the prefetcher generating an access request to a memory when
6 requested by the processor; and

7 a canceler coupled to the storage circuit and the prefetcher
8 to cancel the access request when the access request corresponds
9 to at least P of the stored prefetch addresses, P being a non-zero
10 integer.

1 2. The apparatus of claim 1 wherein the storage circuit
2 comprises:

3 a storage element to store the plurality of prefetch addresses
4 from the most recent access requests by the processor, the storage
5 element being one of a queue with a predetermined size and a
6 content addressable memory (CAM).

1 3. The apparatus of claim 2 wherein the queue comprises:

2 a plurality of registers cascaded to shift the prefetch
3 addresses each time the processor generates an access request.

1 4. The apparatus of claim 3 wherein the canceler
2 comprises:

3 a matching circuit to match a current prefetch address
4 associated with the access request with the stored prefetch
5 addresses.

1 5. The apparatus of claim 4 wherein the canceler further
2 comprises:

3 a cancel generator coupled to the matching circuit to
4 generate a cancellation request to the prefetcher when the current
5 prefetch address matches to the at least P of the stored prefetch
6 addresses.

1 6. The apparatus of claim 4 wherein the matching circuit
2 comprises:

3 a plurality of comparators to compare the current prefetch
4 address with each of the stored prefetch addresses.

1 7. The apparatus of claim 4 wherein the matching circuit
2 comprises:

3 a plurality of comparators to compare the current prefetch
4 address with contents of the plurality of registers, the comparators
5 generating comparison results.

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1 8. (Amended) The apparatus of claim 5 wherein the
2 cancel generator comprises:
3 a comparator combiner coupled to the comparators to
4 combine the comparison results, the combined comparison results
5 corresponding to the cancellation request.

1 9. The apparatus of claim 2 wherein the canceler
2 comprises:
3 a matching circuit having an argument register to store the
4 current prefetch address for matching with entries of the CAM.

1 10. The apparatus of claim 9 wherein the canceler further
2 comprises:
3 a cancellation generator to generate a match indicator when
4 the current prefetch address matches at least P of the entries, the
5 match indicator corresponding to the cancellation request.

1 11. A method comprising:
2 storing a plurality of prefetch addresses in a storage circuit,
3 the plurality of prefetch addresses corresponding to most recent
4 access requests from a processor, the prefetcher generating an
5 access request to a memory when requested by the processor; and

6 canceling the access request when the access request
7 corresponds to at least P of the stored prefetch addresses, P being
8 a non-zero integer.

1 12. The method of claim 11 wherein storing comprises:

2 storing the plurality of prefetch addresses in one of a queue
3 with a predetermined size and a content addressable memory
4 (CAM).

1 13. The method of claim 12 wherein storing the plurality of
2 prefetch addresses in the queue comprises:

3 storing the plurality of prefetch addresses in a plurality of
4 registers cascaded to shift the prefetch addresses each time the
5 processor generates a prefetch request.

1 14. The method of claim 13 wherein canceling comprises:

2 matching a current prefetch address associated with the
3 access request with the stored prefetch addresses.

1 15. The method of claim 14 wherein canceling further
2 comprises:

3 generating a cancellation request to the prefetcher when the
4 current prefetch address matches to the at least P of the stored
5 prefetch addresses.

1 16. The method of claim 14 wherein matching comprises:
2 comparing the current prefetch address with each of the
3 stored prefetch addresses.

1 17. The method of claim 14 wherein matching comprises:
2 comparing the current prefetch address with contents of the
3 plurality of registers, the comparators generating comparison
4 results.

1 18. (Amended) The method of claim 15 wherein
2 generating the cancellation request comprises:
3 combining the comparison results, the combined comparison
4 results corresponding to the cancellation request.

1 19. The method of claim 12 wherein canceling comprises:
2 storing the current prefetch address in an argument register
3 for matching with entries of the CAM.

2 20. (Amended) The method of claim 19 wherein canceling
further comprises:

23
3 generating a match indicator when the current prefetch
4 address matches at least P of the entries, the match indicator
5 corresponding to the cancellation request.

1 21. A system comprising:

2 a processor to generate prefetch requests;

3 a memory to store data; and

4 a chipset coupled to the processor and the memory, the
5 chipset comprising:

6 a prefetcher to generate an access request to the
7 memory when requested by the processor;

8 a prefetch monitor circuit coupled to the prefetcher,
9 the prefetch monitor circuit comprising:

10 a storage circuit coupled to the prefetcher to store a plurality
11 of prefetch addresses, the plurality of prefetch addresses
12 corresponding to most recent access requests from the processor;
13 and

14 a canceler coupled to the storage circuit and the
15 prefetcher to cancel the access request when the
16 access request corresponds to at least P of the stored
17 prefetch addresses, P being a non-zero integer.

1 22. The system of claim 21 wherein the storage circuit
2 comprises:

3 a storage element to store the plurality of prefetch addresses
4 from the most recent access requests by the processor, the storage
5 element being one of a queue with a predetermined size and a
6 content addressable memory (CAM).

1 23. The system of claim 22 wherein the queue comprises:
2 a plurality of registers cascaded to shift the prefetch
3 addresses each time the processor generates an access request.

1 24. The system of claim 23 wherein the canceler
2 comprises:
3 a matching circuit to match a current prefetch address
4 associated with the access request with the stored prefetch
5 addresses.

1 25. The system of claim 24 wherein the canceler further
2 comprises:
3 a cancel generator coupled to the matching circuit to
4 generate a cancellation request to the prefetcher when the current
5 prefetch address matches to the at least P of the stored prefetch
6 addresses.

1 26. The system of claim 24 wherein the matching circuit
2 comprises:

3 a plurality of comparators to compare the current prefetch
4 address with each of the stored prefetch addresses.

1 27. The system of claim 24 wherein the matching circuit
2 comprises:

3 a plurality of comparators to compare the current prefetch
4 address with contents of the plurality of registers, the comparators
5 generating comparison results.

1 28. (Amended) The system of claim 25 wherein the cancel
2 generator comprises:

3 a comparator combiner coupled to the comparators to
4 combine the comparison results, the combined comparison results
5 corresponding to the cancellation request.

1 29. The system of claim 22 wherein the canceler
2 comprises:

3 a matching circuit having an argument register to store the
4 current prefetch address for matching with entries of the CAM.

